type silicon substrate 1, a thick oxide layer, an n-type rectangular region, a transfer gate electrode and an n-type impurity region. Further, the Examiner alleges that Miwada discloses a charge transfer as defined in Claim 1.

To expedite examination and allowance of the application, Applicant has amended Claim 1. Amended Claim 1 defines an active CMOS pixel structure having a semiconductor substrate, a collection region, a dual-purpose electrode, and an amplifier. The semiconductor substrate includes dopants of a first conductivity type at a first concentration density, and an insulating layer at its surface. The collection region includes dopants of a second conductivity type, which is opposite the first conductivity type at a second concentration density, and is formed in the surface region of the semiconductor substrate. The dual-purpose electrode is formed on the insulating layer and extends over both the surface of at least part of the collection region and over at least part of the substrate. The dual-purpose electrode is intended to be driven by a first voltage that causes an electrostatic potential, which collects in an area of the collection region beneath the dual-purpose electrode charges generated by electromagnetic radiation, and by a second voltage, which is higher than the first voltage, for transferring the charges from the collection region into a detection region. The amplifier is integrated in the pixel structure for amplifying the collected charge.

Rejection over Miwada

Applicant respectfully submits that amended Claim 1 is patentably distinguished over Miwada because Miwada does not disclose or suggest each and every limitation recited in amended Claim 1. For example, Miwada does not disclose or suggest an active CMOS pixel structure. Instead, Miwada discloses a CCD structure (see, e.g., column 5, line 39). A CCD pixel structure and a CMOS active pixel structure are completely different devices. In an active pixel structure, incident light is converted into electronic charge within an active pixel. The charge is detected as early as possible by charge sensing amplifiers. In a CCD device, incident light is also converted into electronic charge within each of the CCD pixels. But, after the charge is collected in each pixel, the charge is clocked down each column and into a serial shift register using a method that is often referred to as a "bucket brigade." When the charge reaches the serial shift register, it is transferred perpendicularly along another shift register to one or a plurality of amplifiers.

Accordingly, in Miwada's CCD device, a clock signal CLK is applied to the gate electrode 6c (see Figure 2). Miwada explains in column 5, lines 34-39, that "[a] phase-one transferring clock signal CLK1 and a phase-two transferring clock signal CLK2 are selectively supplied to the gate electrodes 26a to 6h, and the n-type impurity region NR2 and the gate electrodes 26a to 26h as a whole constitute a multi-stage vertical shift register 27 of the CCD type." Therefore, Applicant respectfully submits that Miwada does not disclose an active CMOS pixel structure, as defined in amended Claim 1.

Further, Miwada does not disclose or suggest an active CMOS pixel structure having an amplifier integrated in the pixel structure for amplifying collected charge. Miwada describes the image pick-up device with reference to Figures 1-18. None of these drawings show an amplifier. Further, the specification does not refer to any amplifier. Thus, Miwada's CCD device does not include an amplifier integrated in the pixel structure for amplifying collected charge.

In view of the foregoing, Applicant respectfully submits that Miwada does not anticipate amended Claim 1. Further, Applicant respectfully submits that Miwada provides no suggestion for an active CMOS pixel structure as defined in amended Claim 1. For example, as Miwada is completely silent as to any amplifier, there is no suggestion or motivation to provide an amplifier in Miwada's device. Applicant respectfully requests the Examiner to reconsider the rejection over Miwada and to pass amended Claim 1 to allowance.

Because Claims 2-11 depend from amended Claim 1, pursuant to 35 U.S.C. § 112, ¶ 4, they incorporate by reference all the limitations of the claim to which they refer. It is therefore submitted that these claims are in condition for allowance at least for the reasons expressed with respect to the independent claim, and for their other inventive features. Applicants respectfully request the Examiner to pass Claims 2-11 to allowance.

Rejections over Miwada in view of Kuroda or Hook

The Examiner cited Miwada and Kuroda against dependent Claims 2, 3, 7 and 8, and argues that although Miwada does not disclose a barrier region as defined in Claim 2, Kuroda discloses an image pickup element with p+-type layer as a barrier region. The Examiner concludes that it would have been obvious to include the p+-type layer underneath the n-type

diffused layer of Miwada to direct charges to the pn junction and reduce smearing, as thought by Kuroda.

Applicant respectfully disagrees with the Examiner's conclusion and submits that a combination of Miwada and Kuroda does not disclose or suggest each and every limitation recited in Claims 2, 3, 7 and 8, which depend from amended Claim 1. This applies even though Kuroda discloses that the CCD device includes a p+-type layer 13 and a p-type layer 16, and a potential barrier against the charge 14 is formed around the depletion layer 11 (col. 2, lines 56-64). Thus, one of ordinary skill in the art would not combine Kuroda and Miwada in a way asserted by the Examiner.

In order to provide a *prima facie* showing of obviousness, the Patent and Trademark Office has the burden to provide a motivation, teaching, or suggestion to create the claimed invention. *See, e.g., In re Fine*, 5 U.S.P.Q.2d 1597 (Fed. Cir. 1988). Moreover, the evidence to prove the motivation, teaching, or suggestion must be clear and particular and can flow from three sources: (1) the prior art references themselves, (2) the knowledge of one of ordinary skill in the art, or (3) from the nature of the problem to be solved. *See In re Dembiczak*, 175 F.3d 994, 999 (Fed Cir. 1999). Thus, a rejection cannot be predicated on the mere identification of individual components of claimed limitations ("mosaicing"). The particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components in the manner claimed. *See In re Kotzab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000).

In the case of the presently claimed invention, Applicant respectfully submits that none of these evidentiary sources exist to provide such a motivation, teaching or suggestion. First, the prior art references themselves do not disclose an active CMOS pixel structure, even if combined. As discussed above with reference to amended Claim 1, Miwada does not disclose an active CMOS pixel structure, but discloses a CCD pixel structure. Kuroda discloses an image pickup device having a CCD device (e.g., Abstract). Second, those of ordinary skill in the art would not be motivated to integrate an amplifier in a CCD device in view of the complete absence of an amplifier in the devices of the cited prior art. And third, the nature of the problem

to be solved in the prior art does not suggest a motivation to integrate an amplifier in a CCD device.

With respect to the latter, Applicant notes that Miwada emphasizes the problem of after images in the prior art (column 2, line 21 to column 3, line 35). Miwada achieves a reduction of after images by adjusting the ratio of parallel segments W1 and W2 of a trapezoidal configuration to a specifically selected value (column 6, lines 42-51). Miwada does not require an amplifier. Thus, even a combination of Miwada and Kuroda does not disclose or suggest each and every limitation of the claimed subject matter.

The Examiner cited Hook against dependent Claims 9-11, and argues that although Miwada does not disclose a pinning region, Hook discloses an active pixel sensor cell having a pinning region. The Examiner concludes that it would have been obvious to include the pinning region of Hook in Miwada's device to improve the collection and retention of electrons within the n-type diffused layer.

In view of the requirements for a *prima facie* showing of obviousness set forth above, Applicant respectfully disagrees with the Examiner's conclusion and submits that a combination of Miwada and Hook does not disclose or suggest each and every limitation recited in Claims 9-11, which depend from amended Claim 1. More particularly, Miwada does not disclose an active pixel structure as recited in Claim 1, but discloses a CCD pixel structure. Hook discloses an active pixel comprising two electrodes 24 and 24'. Hook also discloses a pinning region. However, including the pinning region as described in Hook into Miwada's device does not lead to an active CMOS pixel structure defined in amended Claim 1.

New Claim 12

Claim 12 has been added to define that the barrier region of Claim 2 substantially impedes the diffusion of charges to the second region. Claim 12 depends from Claim 2, which depends from Claim 1, and pursuant to 35 U.S.C. § 112, ¶ 4, incorporates by reference all the limitations of the claim to which it refers. It is therefore submitted that Claim 12 is in condition for allowance at least for the reasons expressed with respect to the independent claim, and for its other inventive features. Applicants respectfully request the Examiner to pass Claim 12 to allowance.

Summary

Applicant believes that none of the prior art references appear to disclose each and every claimed limitation. Moreover, none of the prior art references would even suggest angles within the presently claimed range because the problem referred to above of reducing the empty space was only identified by the Applicant in connection with the invention of the present application.

In view of the foregoing, Applicant respectfully requests the Examiner to withdraw the rejections over Miwada, Kurada and Hook and to pass Claim 1 as amended to allowance. Claims 2-12 depend directly or indirectly from Claim 1 and further define the invention of Claim 1 as amended. Thus, for the reasons set forth above and because of the inventive features of Claims 2-12, Applicant respectfully submits that Claims 2-12 are patentably distinguished over the prior art and respectfully request the Examiner to pass Claims 2-12 to allowance.

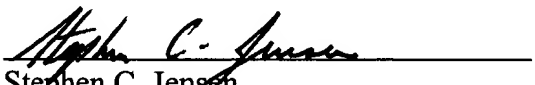
CONCLUSION

Applicant has endeavored to address all of the Examiner's concerns as expressed in the outstanding Office Action. In light of the above remarks, reconsideration and withdrawal of the outstanding rejections is specifically requested. If the Examiner finds any remaining impediment to the prompt allowance of these claims that could be clarified with a telephone conference, the examiner is respectfully requested to initiate the same with the undersigned.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: Nov. 12, 2002

By: 

Stephen C. Jensen
Registration No. 35,556
Attorney of Record
Customer No. 20,995
(949) 760-0404

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 1 has been amended as follows:

1. (Thrice Amended) An active ~~or passive~~ CMOS pixel structure comprising:

a semiconductor substrate with dopants of a first conductivity type at a first concentration density, and with an insulating layer at its surface;

a collection region with dopants of a second conductivity type which is opposite the first conductivity type at a second concentration density, formed in the surface region of the semiconductor substrate;

a dual-purpose electrode formed on the insulating layer, extending over both the surface of at least part of the collection region and over at least part of the substrate, the dual-purpose electrode being intended to be driven by a first voltage that causes an electrostatic potential which collects in an area of the collection region beneath the dual-purpose electrode charges generated by electromagnetic radiation and by a second voltage, which is higher than the first voltage, for transferring the charges from the collection region into a detection region, and

an amplifier integrated in the pixel structure for amplifying the collected charge.